REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application.

I. REAL PARTY IN INTEREST

The present Application is assigned to Altera Corporation, a Delaware corporation, as indicated by an assignment from the inventors recorded on April 22, 2004 in the Assignment Records of the United States Patent and Trademark Office at Reel 015261, Frame 0003.

II. RELATED APPEALS AND INTERFERENCES

Applicants, the undersigned Attorney, and Assignee are not aware of any related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in an appeal of this application.

III. STATUS OF CLAIMS

Claims 1, 3, and 5-22 in the present application are pending.

Claim 3 has been amended.

Claims 1, 3, and 5-22 are rejected under 35 U.S.C. § 101.

Claims 1, 3, 5-7, 9, and 11-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,711,602 ("Bhandal") in view of U.S. Patent No. 7,046,723 ("Schier").

IV. STATUS OF AMENDMENTS

Claim 3 has been amended. Support for the amendment to claim 3 is found in claim 2 as originally filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

With respect to independent claim 1, a method for performing multiplication on a field programmable gate array includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers (see paragraph [0026] and Figure 1). A stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number is retrieved from a memory (see paragraph [0026]). The product is scaled with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (see paragraph [0027]). A scaled product and a scaled stored value is summed to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits (see paragraph [0027]).

With respect to independent claim 11, a method for implementing a multiplier on a field programmable gate array includes configuring a digital signal processor (DSP) to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (see paragraph [0026] and Figure 1). Products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number are stored in a memory (see paragraphs [0026]-[0027] and [0029]-[0030] and Figures 1 and 2). An output is routed from the DSP to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (see paragraph [0055] and Figures 7 and 8). An output is routed out of the memory to the adder such that the output from the memory is scaled according to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (see paragraphs [0055]-[0056] and Figures 7 and 8). A value representing a product of the first and second number where the first and second number each have more than the first plurality of bits is output, wherein the DSP is configured to support multiplication of no more than the first plurality of bits (see paragraphs [0005] and [0056] and Figures 7 and 8).

With respect to independent claim 17, a multiplier includes a digital signal processor (DSP) configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (see paragraphs [0005] and [0026] and Figure 1). The multiplier includes a memory that stores products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (see paragraphs [0026]-[0027] and [0029]-[0030] and Figures 1 and 2). The multiplier includes an adder that sums a scaled output of the DSP and a scaled output of the memory to output a value representing a product of the first and second number where the first and second number each have more than the first plurality of bits, wherein the DSP is only configurable to support multiplication of a number of bits equal to or less than the first plurality of bits (see paragraphs [0005] and [0055]-[0056] and Figures 7 and 8).

With respect to independent claim 21, a method for implementing a multiplier on a field programmable gate array includes configuring a digital signal processor (DSP) to perform multiplication on a first n bits from a first number and a first n bits from a second number (see paragraph [0026] and [0028] and Figures 1 and 2). Products resulting from multiplication of a second m bits from the first number and a second m bits from the second number are stored in a memory (see paragraphs [0026]-[0027] and [0029]-[0030] and Figures 1 and 2). An output from the DSP to an adder is routed such that the output from the DSP is scaled according to a position of the first n bits from the first number and a position of the first n bits from the second number (see paragraph [0055] and Figures 7 and 8). An output of the memory is routed to the adder such that the output from the memory is scaled according to a position of the second m bits from the first number and a position of the second m bits from the second number (see paragraphs [0055]-[0056] and Figures 7 and 8). A value representing a product of the first and second number is routed where the first and second number each have at least n + m number of bits (see paragraphs [0005] and [0056] and Figures 7 and 8).

With respect to independent claim 22, a multiplier includes a digital signal processor (DSP) configured to perform n*n multiplication on a first plurality of n bits from a first number and a first plurality of n bits from a second number (see paragraphs [0005] and [0026] and Figure 1). The multiplier includes a memory that stores products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (see paragraphs [0026]-[0027] and [0029]-[0030] and Figures 1 and 2). The multiplier includes an adder that sums a scaled output of the DSP and a scaled output of the memory to output a value representing a product of the first and second number where the first and second number each have more than n bits (see paragraphs [0005] and [0055]-[0056] and Figures 7 and 8).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Were claims 1-3, and 5-22 properly rejected under 35 U.S.C. §101 as being directed to non-statutory matter?

2. Were claims 1-3, 5-7, 9, and 11-22 properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,711,602 ("Bhandal") in view of U.S. Patent Number 7,046,723 ("Schier")?

3. Was claim 18 properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,711,602 ("Bhandal") in view of U.S. Patent Number 7,046,723 ("Schier")?

VII. ARGUMENT 1

Claims 1-3, and 5-22 were improperly rejected under 35 U.S.C. § 101.

The Office Action mailed 4/1/2008 states in part that

> Claims 1, 3 and 5-22 cite a method and device performing multiplication with a predetermined mathematical algorithm. However, claims 1, 3, and 5-22 merely disclose series of steps for performing sum of shift products without further disclosing a practical application. In addition, claims 1, 3, and 5-22 appear to preempt every substantial practical application of the idea embodied by the claims. Therefore, claims 1, 3 and 5-22 are directed to non-statutory subject matter.

(4/1/2008 Office Action, p. 1).

This rejection is respectfully traversed for the following reasons.

Applicants submit that Claims 1, 3, and 5-22 cover a practical application of a judicial exception. As noted in the M.P.E.P.,

> A claimed invention is directed to a practical application of a 35 U.S.C. §101 judicial exception when it:
> (A) "transforms" an article or physical object to a different state or thing; <u>or</u>
> (B) otherwise produces a useful, concrete and tangible result, based on the factors discussed below.

(M.P.E.P. § 2106(IV)(C)(2)) (Emphasis Added).

According to M.P.E.P. § 2106(IV)(C)(2)(1), the inquiry into whether a claim covers a practical application of a 35 U.S.C. 101 judicial exception begins with a threshold determination.

M.P.E.P. § 2106(IV)(C)(2)(1) states:

> USPTO personnel first shall review the claim and determine if it provides a transformation or reduction of an article to a different state or thing. If USPTO personnel find such a transformation or reduction, USPTO personnel shall end the inquiry and find that the claim meets the statutory requirement of 35 U.S.C. 101. If USPTO personnel do not find such a transformation or reduction, they must determine whether the claimed invention produces a useful, concrete, and tangible result.

Claims 1, 3, and 5-10 Transform an Article to a Different State

Applicants submit that the method of Claim 1 transforms and reduces articles to a different state or thing. Claim 1 recites a method for performing multiplication on a field programmable gate array. The method includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits than those forming the first and second numbers. A stored value designated as a product of second plurality of bits from the first number and a second plurality of bits from the second number is retrieved from a memory. The product is scaled with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and the stored value is scaled with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number. A scaled product and a scaled stored value is summed to generate a value equivalent to a product of the first and second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

Applicants submit that "generating a product by multiplying… using a digital signal processor (DSP)", "retrieving a store value", "scaling the product … and scaling the stored value", and "summing a scaled product and a scaled stored value to generate a value representing a product of the first and second numbers", provide transformation or reduction of an article to a different state or thing. The first and second numbers have been transformed by virtue of the method of Claim 1 to a different, generated value representing the product. Thus, because the method of Claim 1 transforms an article to a different thing, Applicants believe that Claim 1 is directed to statutory subject matter under 35 U.S.C. § 101.

Claims 1, 3, 5-10, and 22 Produce a Useful, Tangible, and Concrete Result

Furthermore, to meet the requirements of 35 U.S.C. § 101, "[t]he claimed invention as a whole must accomplish a practical application. That is, it must produce a 'useful, concrete and tangible result.'" M.P.E.P. § 2106(II)(A) (quoting State Street Bank & Trust v. Signature Financial Group, Inc., 149 F.3d 1368, 1373, 47 USPQ2d 1596, 1601 (Fed. Cir. 1998)). State Street provides the following example of a claimed invention that produces a useful, concrete, and tangible result:

> [T]ransformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces 'a useful, concrete and tangible result' – a final share price momentarily fixed for recording and reporting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades.

State Street, 149 F.3d at 1373, 47 USPQ2d at 1601.

It is respectfully submitted that if "transformation of data. . .into a final share price" is statutory subject matter, as in the State Street case, then the method of Claim 1 is also statutory because it constitutes a practical application to produce a "useful, concrete, and tangible result", i.e., the value representing a product of the first and second number, wherein the first and second number each have a number of bits equal to or greater than the total of the first and second number of bits. By virtue of the method of Claim 1, the product of the two numbers can be obtained by the field programmable gate array despite the fact that the DSP of the array is capable of multiplying only a fewer number of bits than those forming the two numbers. As such, the result of the method clearly is "useful, concrete, and tangible" in that it is achieved without having to employ a DSP capable of multiplying at least the total number of bits of the two numbers.

For these reasons, Claim 1, as well as the claims dependent there from, are believed to clearly recite statutory subject matter.

Claims 22 include subject matter similar to that of Claims 1, 3, and 5-10 and therefore are submitted to be directed to patentable subject matter for the same reasons. Therefore, withdrawal of the rejections is respectfully requested.

Claims 11-21 Transform an Article to a Different State

Applicants also submit that the method of Claim 11 transforms and reduces articles to a different state or thing. Claim 11 recites a method for implementing a multiplier on a field programmable gate array. The method includes configuring a digital signal processor to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number. Products are stored resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number in a memory. An output from the DSP is routed to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number. An output of the memory is routed to the adder such that the output from the memory is scaled according to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number. A value representing a product of the first and second number is output where the first and second number each have more than the first plurality of bits, wherein the DSP is configured to support multiplication of no more than the first plurality of bits.

Applicants submit that "configuring a digital signal processor (DSP) to perform multiplication", "storing products resulting from multiplication", "routing an output from the DSP to an adder such that the output from the DSP is scaled", "routing an output of the memory to the adder such that the output from the memory is scaled", and "outputting a value..." provide transformation or reduction of an article to a different state or thing. The DSP, memory, routing from the DSP to adder, and routing from the memory to the adder on the field programmable gate array have clearly been transformed. Thus, because the method of Claim 11 transforms the components on the field programmable gate array to a different state by "routing an output from the DSP to an adder such that the output from the DSP is scaled" and "routing an output of the memory to the adder such that the output from the memory is scaled", Applicants submit that Claim 11 is directed to statutory subject matter under 35 U.S.C. § 101. Furthermore, Applicants submit that the DSP, memory, routing from the DSP to adder, and routing from the memory to the adder on the field programmable gate array also transform the first number and second number to a value representing a product of the first and second numbers, despite the fact that the DSP is configured to support multiplication of no more than the first plurality of bits. Thus because the method of Claim 11 transforms the first and second numbers to a different state, Applicants submit that Claim 11 is directed to statutory subject matter under 35 U.S.C. § 101.

Claims 11-21 Produce a Useful, Tangible, and Concrete Result

As stated above, in the State Street decision, the Court of Appeals for the Federal Circuit held that "transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price constitutes a practical application … … because it produces 'a useful, concrete, and tangible result'". Applicants respectfully submit that the method of Claim 11 comprising, inter alia, outputting a value representing a product of a first and second number where the first and second number each have more than a first plurality of bits, but wherein a DSP is configured to support multiplication of no more than the first plurality of bits as described in Claim 11, similarly represent statutory subject matter under 35 U.S.C. § 101. That is, the configuring of a DSP, storing of products in a memory, routing of an output from the DSP to an adder, routing of an output from the memory to an adder, and outputting provide a "useful, concrete, and tangible result", i.e., a value representing a product of a first and second number where the first and second number each have more than the first plurality of bits. The product of the two numbers is obtained by the field programmable gate array despite the fact that the DSP of the array is capable of supporting multiplication of no more than the first plurality of bits, and thus it is not necessary to employ a DSP capable of multiplying more that that number of bits.

For these reasons, Claim 11 as well as the claims dependent there from are believed to clearly recite statutory subject matter as well.

Claims 17-21 include subject matter similar to that of Claims 11-16 and therefore are submitted to be directed to patentable subject matter for the same reasons. Therefore, withdrawal of the rejections is respectfully requested.

VIII. ARGUMENT 2

Claims 1, 3, 5-7, 9, and 11-22 were improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over 6,711,602 ("Bhandal") in view of U.S. Patent 7,046,723 ("Schier").

It is submitted that Bhandal and Schier do not render claims 1, 3, 5-7, 9, and 11-22 unpatentable under 35 U.S.C. §103(a).

Bhandal includes a disclosure of a pair of parallel 16.times.16 multipliers each with two 32-bit inputs and one 32-bit output. There are options to allow input halfword and byte selection for four independent 8x8 or two independent 16x16 multiplications, real and imaginary parts of complex multiplication, pairs of partial sums for 32x32 multiplication, and partial sums for 16x32 multiplication. There are options to allow internal hardwired routing of each multiplier unit results to achieve partial-sum shifting as required to support above options. There is a redundant digit arithmetic adder before final outputs to support additions for partial sum accumulation, complex multiplication vector accumulation and general accumulation for

FIRs/IIRs--giving MAC unit functionality. There are options controlled using bit fields in a control register passed to the multiplier unit as an operand. There are also options to generate all of the products needed for complex multiplication (see Bhandal Abstract).

Schier includes a disclosure of a digital and a multiplication method are described, which lead to an efficient architecture for a hardware implementation of digital FIR and IIR filters into FPGAs. The multiplications of input sample data and delayed sample data with filter coefficients are performed by addressing look-up tables in which corresponding multiplication results are prestored. The size of the look-up tables is reduced by storing only those multiplication results which cannot be obtained by a shifting operation performed on the other pre-stored multiplication results, the input sample data, or the delayed sample data. Thereby, the size of the look-up tables can be compressed significantly such that an implementation of large digital filters into FPGAs is possible (see Schier Abstract).

It is submitted that Bhandal and Schier do not teach or suggest a method for performing multiplication on a field programmable gate array that includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers, retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory, scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number, and summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits cqual to or greater than a total of the first and second plurality of bits.

The Examiner acknowledges that Bhandal does not disclose retrieving a stored value designated as a product of a second plurality of bits from a first number and a second plurality of bits from a second number from memory.

With respect to Claims 1 and 21, the Examiner has stated in part that

> Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).
>
> Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3, lines 9-11 and col. 4, lines 9-12).

(4/1/2008 Office Action, p. 4 and 11).

Applicants submit, however, that Schier teaches away from a combining a DSP biased multiplier such as that described in Bhandal with an FPGA biased multiplier such as that described in Schier. Schier discloses a digital filter that includes a look-up table (LUT) based multiplier 2 (see Figure 1). The digital filter disclosed in Schier is implemented on a field programmable gate array (FPGA) (see Schier column 4, lines 3-12 and column 9, lines 6-19). Schier points out that digital filters have distinct architectures used for implementation and that these architectures fall into one of three categories: digital signal processors, application specific integrated circuits, *or* field programmable gate arrays. Schier specifically states

> The performance of the digital filter depends on the architecture used for implementation, i.e. DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) *or* FPGA (Field Programmable Gate Array).

(Schier column 1, lines 28-31) (Emphasis Added).

Clearly, Schier intends for a digital filter to have an architecture from only one of the three groups listed and thus teaches away from combining the DSP based architecture of Bhandal with the FPGA based architecture of the digital filter described in Schier.

Furthermore, Applicants submit that "the intermediate product from the LUT in Figures 1-4" of Schier cannot be arbitrarily used as "the second product" as the Examiner suggests on page 4 of the Office Action mailed 4/1/2008. The Examiner states that both the product generated by the DSP and the stored value from memory are scaled in Bhandal by the shifters 810 and 811 illustrated in Figure 8.

> Re claim 1, Bhandal et al. disclose in Figures 1-22 a method for performing multiplication (e.g. abstract and Figure 8 as general architecture of multiplier), comprising: generating a product by multiplying a first plurality of bits from a first number and a second plurality of bits from a second number (e.g. Figure 11B wherein SRC1_L as B is multiplying with SRC2_L as D by B*D) using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers (e.g. by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands); a product of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11 wherein SRC1_H as A is multiplying with SRC2_H as C by A*C); scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8) and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8); and summing a scaled product and a sealed (sic) stored value to generate a value representing a product of the first number and the second number (e.g. output of adder 820 in Figure 8 and Figure 11B), wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits (e.g. Figure 11B wherein each of input operands consist of 32 bits and each of input multiplied operand is 16 bits).

(4/1/2008 Office Action, pp. 3-4) (Emphasis Added).

Applicants submit that the Schier discloses a filter with a LUT based multiplier where additional shifting operations are not performed after multiplications. Schier specifically states

> Moreover, since the input sample data is not divided into its bit positions, an additional shifting operation is not required after the multiplications and a low latency is introduced.

(Schier column 4, lines 3-6).

Thus, clearly Schier does not permit the shifting which the Examiner is requiring for the "stored value" by shifter 811 in Figure 8 of Bhandal.

By combining Bhandal and Schier, the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose. Applicants submit that when this is the case, there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900 (Fed. Cir. 1984). Applicants further submit that it is improper to combine references where the references teach away from their combination. In re Grasselli, 713 731, 743 (Fed. Cir. 1983).

In contrast, claim 1 states

> A method for performing multiplication on a field programmable gate array, comprising:
>
> generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers;
>
> retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory;
>
> scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number; and
>
> summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of

> bits equal to or greater than a total of the first and
> second plurality of bits.

(Claim 1) (Emphasis Added).

Claims 11, 17, 21, and 22 include similar limitations.

Given that claims 3, and 5-10 depend from claim 1, claims 12-16 depend from claim 11, and claims 18-20 depend from claim 17, it is likewise submitted that claims 3, 5-10, 12-16, and 18-20 are also patentable under 35 U.S.C. §103(a) over Bhandal and Schier.

IX. ARGUMENT 3

Claim 18 was improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over 6,711,602 ("Bhandal") in view of U.S. Patent 7,046,723 ("Schier").

It is submitted that Bhandal and Schier do not render claim 18 unpatentable under 35 U.S.C. §103(a).

It is submitted that Bhandal and Schier do not teach or suggest a multiplier that includes a digital signal processor (DSP) configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number, a memory that stores products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number, and an adder that sums a scaled output of the DSP and a scaled output of the memory to output a value representing a product of the first and second number where the first and second number each have more than the first plurality of bits, wherein the DSP is only configurable to support multiplication of a number of bits equal to or less than the first plurality of bits, wherein the DSP, the memory, and the adder reside on a field programmable gate array.

The Examiner states in part that

> Re claim 18, Bhandal et al. fail to disclose in Figures 1-22 the DSP, the memory, and the adder reside on a field programmable gate array. However, Schier et al. disclose in Figures 1-4 the

> DSP, the memory, and the adder reside on a field programmable gate array (e.g. abstract).

(4/1/2008 Office Action, p. 9)

Applicants disagree. As stated above, Schier discloses a digital filter that includes a look-up table (LUT) based multiplier 2 (see Figure 1). The digital filter disclosed in Schier is implemented on a field programmable gate array (FPGA) (see Schier column 4, lines 3-12 and column 9, lines 6-19). Schier points out that digital filters have distinct architectures used for implementation and that these architectures fall into one of three categories: digital signal processors, application specific integrated circuits, ***or*** field programmable gate arrays. Schier specifically states in part

> The performance of the digital filter depends on the architecture used for implementation, i.e. DSP (Digital Signal Processor), ASIC (Application Specific Integrated Circuit) ***or*** FPGA (Field Programmable Gate Array).

(Schier column 1, lines 28-31) (Emphasis Added).

Clearly, Schier intends for a digital filter to have an architecture from only one of the three groups listed and thus teaches away from combining the DSP based architecture of Bhandal with the FPGA based architecture of the digital filter described in Schier.

The Examiner cites the Abstract of Schier as support that "the DSP, the memory, and the adder reside on a field programmable gate array". However, the Abstract of Schier makes absolutely no mention of a DSP on a field programmable gate array. Furthermore, the only reference to a DSP in the entire Schier patent is made to distinguish a DSP architecture from an FPGA architecture, not to describe having a DSP reside on an FPGA (see Schier column 1, lines 28-31). Applicants respectfully request that the Examiner clarify the relevance of the cited reference.

In contrast, claim 18 states

> The multiplier of Claim 17, wherein the DSP, the memory, and the adder reside on a field programmable gate array.

(Claim 18) (Emphasis Added).

In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1, 3, and 5-22 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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